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DISCLOSURE TITLE: Fabricating One Semiconductor Contact Stud Borderless to
Another.

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DISCLOSURE TEXT:

- To accommodate future DRAM density considerations (density may require node strap contacts and bit line contacts to overlap), a method is shown for fabricating one contact stud borderless to another so as to maintain electrical isolation.

- A contact borderless to a gate is well known; however, one contact borderless to another is new, i.e., a neighboring contact is defined, etched, and filled, borderless to an existing contact. The existing contact requires an etch-resistant sidewall spacer, and optionally also an etch-resistant cap if the contact material itself is not etch- resistant. Extensions to this technique include borderless gate to diffusion contacts and two borderless vias, one borderless to another.

- A borderless diffusion contact is shown (Fig. 1) borderless to a node connection defined as the overlap. The basis for isolation between these two contacts is the sidewall insulation and insulator cap. Two processing methods are shown to obtain sidewall and top insulators.

Method 1

Referring to Fig. 2, after the polysilicon mandrel is applied, the node contact hole is defined (masked and etched). Oxide or a similar insulator is deposited conformally and reactive ion etched (RIE) back to form spacers. Next, the polysilicon strap material is deposited conformally and recessed back to height "X". It should be noted that the oxide or nitride mask used to etch the intrinsic polysilicon mandrel is left in place to serve as a RIE resistant mask for the polysilicon strap etch. An insulator material is then conformally deposited to fill the node contact opening left. The

diffusion contact mask is used to etch the oxide down to the intrinsic polysilicon mandrel surface with some overetch, thickness "Y" in Fig. 3. After the mask is removed, the diffusion contact opening hole left is filled with metal, e.g., TiN/CVD-W, and oxide is blanket RIE'd back and overetched again to "Y" overetch. The mandrel is then stripped (Fig. 4), leaving the structure to be filled with oxide or other insulator.

Method 2

This method is identical to method 1, except the polysilicon mandrel is replaced with high temperature polyimide and the oxide cap is replaced with an A1100 copolymer spin on glass. In method one, two contacts are made borderless to each other; however, these contacts connect three different conductors, i.e., the node or strap stud contacts trench to diffusion and the diffusion stud contacts metal level zero (Md) to diffusion. A cap and sidewall on the strap stud is necessary due to the overlay of the diffusion stud and strap stud (Fig. 5). With method 2, stud 1 is defined, but a spacer of a different material is added. Stud 1 is filled and then planarized. Next, stud 2 is defined, but when the insulator is etched, the stud 1 surface and spacer is not etched. Stud 2 is filled and planarized. Note that now stud 1 and stud 2 are isolated from each other and serve to connect metal level one (M1) to Md, both on pitch (Fig. 6).

FIG. 1

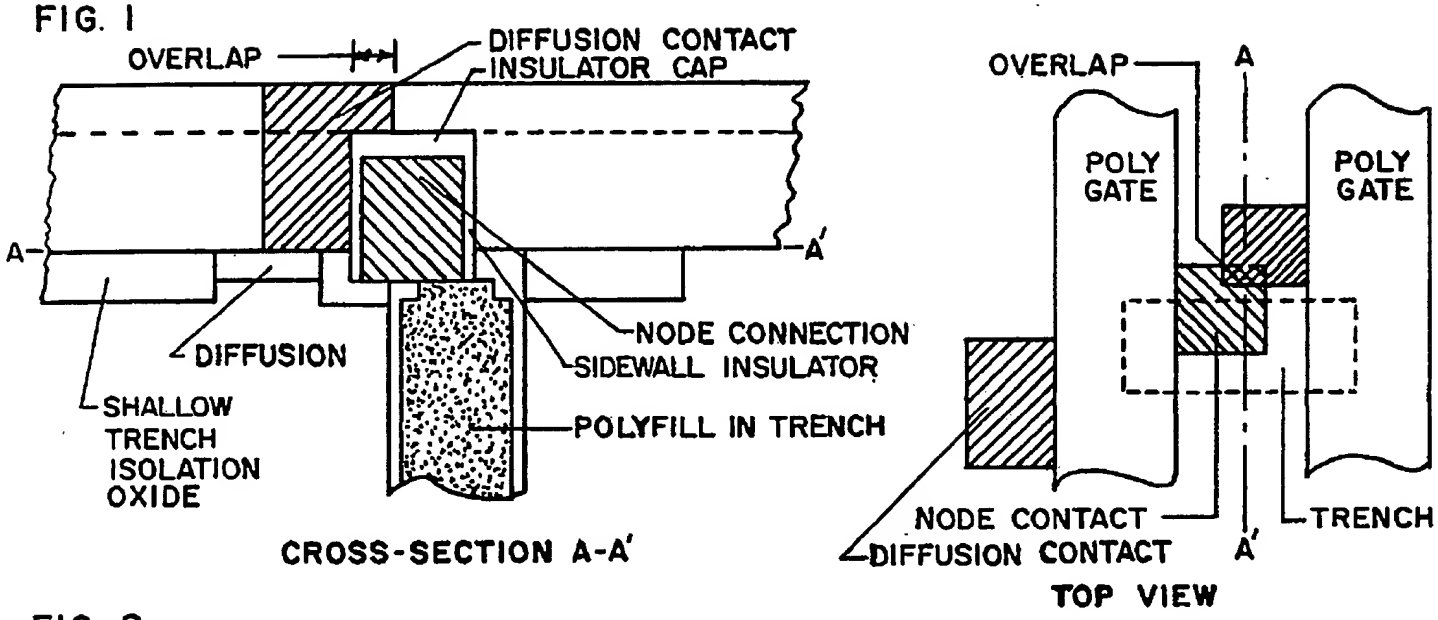

FIG. 2

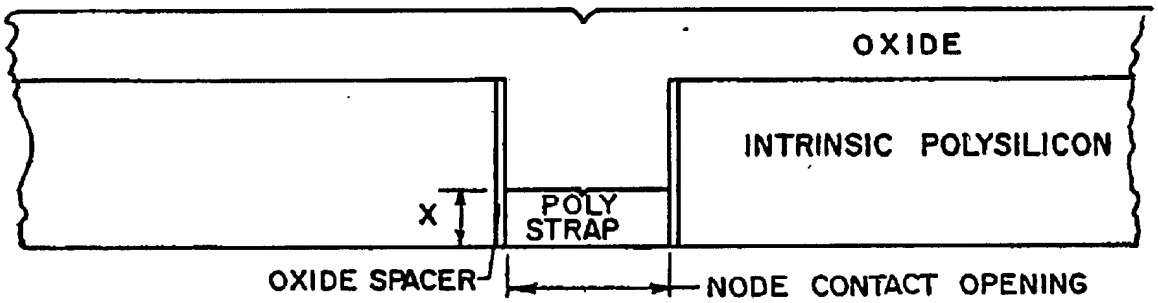

FIG. 3

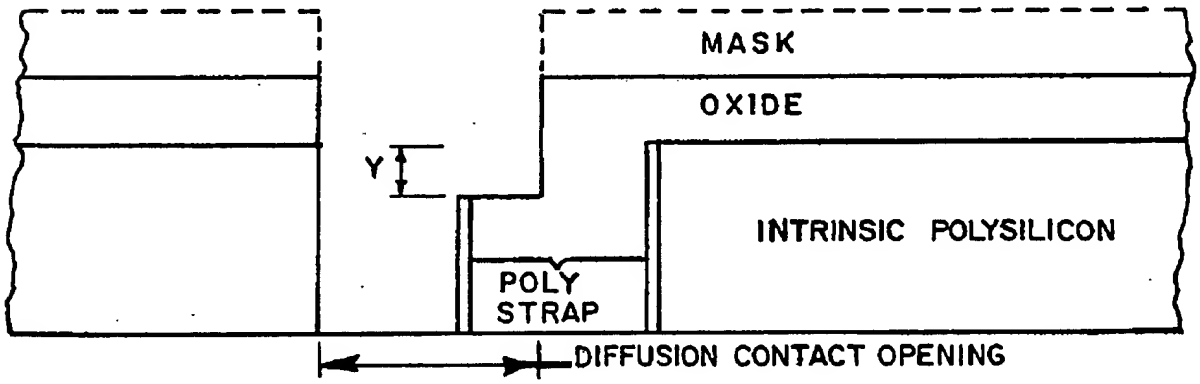

FIG. 4

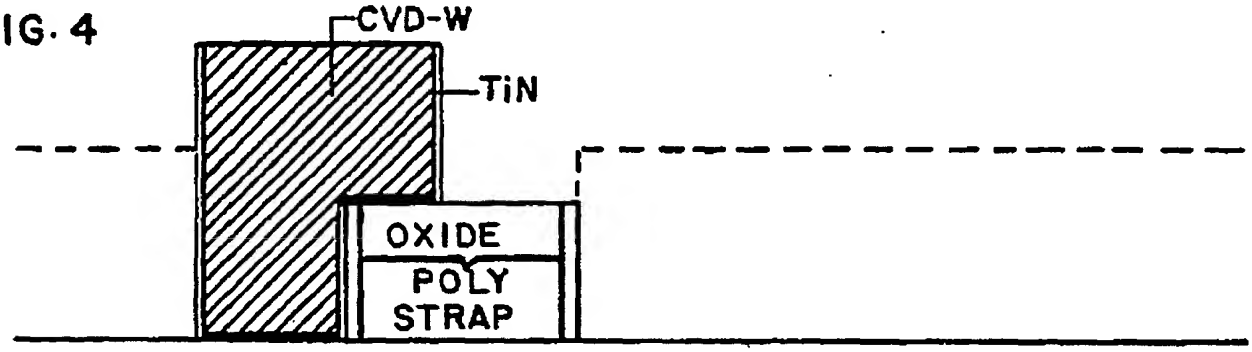

FIG. 5

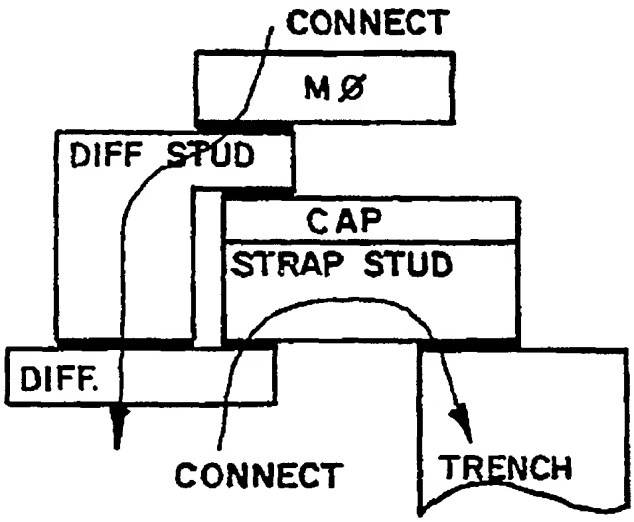

FIG. 6